# UNITED STATES PATENT APPLICATION

of

**Lewis B. Aronson,**

**Rudy Hofmeister,**

**Christopher Madden,**

**Mark Farley,**

**Dan Case,**

**and**

**Tom Lenosky**

for

## INTEGRATED CIRCUIT WITH DUAL EYE OPENERS

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Inventors

Lewis B. Aronson
Rudy Hofmeister
Christopher Madden
Mark Farley
Dan Case
Tom Lenosky

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001]    This application is a divisional of U.S. Patent Application Serial No. 10/420,027, "Transceiver Module and Integrated Circuit With Dual Eye Openers," filed April 17, 2003, which claims the benefit of U.S. Provisional Patent Application Serial No. 60/410,509, filed September 13, 2002 and which also claims the benefit of U.S. Provisional Patent Application Serial No. 60/391,877, filed June 25, 2002. The foregoing patent applications are incorporated herein by reference in their entirety.

## BACKGROUND

### A.    Technical Field

[0002]    The present invention relates generally to ensuring data integrity within a networking box, and more particularly, to on-chip clock and data recovery in a transceiver module.

B.    Background of the Invention

[0003]        The proliferation and significance of networking technology is well known. The ever-increasing demand for network bandwidth has resulted in the development of technology that increases the amount of data traveling across a network.  Advancements in modulation techniques, coding algorithms and error correction have drastically increased rates of this data.  For example, a few years ago, the highest rate that data could travel across a network was at approximately one Gigabit per second (Gb/s).  This rate has increased ten-fold today where data travels across Ethernet and SONET (Synchronous Optical Network) networks at upwards of 10Gb/s.  For instance, the XFP (10 Gb/s serial electrical interface) Pluggable Module Multi-Source Agreement is directed at transceivers operating at approximately 10 Gb/s.

[0004]        Figure 1 illustrates some of the shortcomings of a transceiver module 100 commonly used in prior art networking devices.  The transceiver module 100 is coupled to a network via interfaces 130, 135 and to a host device 105 such as a media access controller ('MAC') card or SONET framer.  The transceiver module 100 has a receiver 115 that is coupled to network interface 130 and a first serializer/deserializer ('SERDES') 110.  The first SERDES 110 is coupled to the host 105 via a parallel bus 140.  An example of this parallel bus 140 may be a (XAUI) 10-Gigabit Attachment Unit Interface that has four 3.125 Gb/s channels that transfer an aggregate 10 Gb/s data stream between the transceiver module 100 and the host 105.  The transceiver module 100 also has a transmitter 125 that is coupled to network interface 135 and a second SERDES 120.  The second SERDES 120 is coupled to the host 105 via a second parallel bus 145 such as the XAUI described above.

[0005]        In operation, a serial optical data stream received by the transceiver module 100 is converted to an electrical serial data stream by the receiver 115.  This electrical serial data

2                                                      20600/06872/1343407

stream is deserialized by the SERDES 110 into four channels and transmitted via the parallel bus

140 to the host 105 for processing. This deserialization occurs in order to prevent further

bandwidth degradation of the electrical data stream and stay below a jitter budget as it continues

to travel along the data path. A high data rate electrical signal (e.g., 10 Gb/s) is more easily

distorted by imperfections within the data path and by the inductance of the bus and connections

along the data path. Reflections caused by discontinuities within a transmission line and

amplitude degradations caused by nodes within a path (e.g., wire bond, solder bump, etc.) may

significantly increase errors within the signal and increase jitter beyond an acceptable threshold

or budget. Additionally, inductance is proportionally more severe at higher frequencies. Thus,

the data stream is deserialized onto parallel transmission lines in order to reduce the rate on each

of these lines and minimize degradation along the data path.

[0006]     A similar deserialization occurs on the transmit side of the transceiver

module 100 for the same reasons described above. In particular, a deserialized electrical data

stream is transferred from the host 105 to the second SERDES 120 via parallel bus 145. The

second SERDES 120 serializes this electrical signal. The transmitter 125 converts the serial

electrical signal to an optical signal and transmits it onto the network.

[0007]     One drawback of module 100 is that the SERDES 110, 120 and the

interfaces to the parallel buses 140, 145 require a relatively large amount of space on the

transceiver module 100. Additionally, SERDES consume power and release a relatively large

amount of heat. Another drawback of module 100 is that conventional transceiver modules do

not include convenient, cost-effective means to monitor the status of data paths and confirm

proper operation of the transceiver.

[0008]     Fiberoptic modules operating at data rates less than 10 Gb/s commonly employ serial electrical interfaces without any means of resetting the jitter budget at the inputs and outputs of the module 100. The most common data rates for these modules are at 1.0625 Gb/s for Fibre Channel, 1.25 Gb/s for Gigabit Ethernet, 2.125 Gb/s for double-rate Fibre Channel, 2.48 Gb/s for OC-48, 2.7 Gb/s for forward error correction ('FEC') rates of OC-48, and numerous rates less than 1 Gb/s for other applications. Serial modules are also used for proprietary links at data rates from less than 1 Gb/s to about 3.125 Gb/s. At these relatively low data rates, there is no need to perform reshaping or retiming of the data at the electrical inputs and outputs ('I/Os') of the module because the signal degradations at those data rates are sufficiently small. However, at data rates approaching or exceeding 10 Gb/s, the bit periods become sufficiently short so that signal degradations are difficult to minimize using conventional approaches to serial modules. Additionally, serial modules at data rates lower than 10 Gb/s can have digital or analog monitoring functions, but the types of error monitoring or diagnostic features that are possible in a module incorporating an integrated SERDES have not thus far implemented.

[0009]     Moreover, the XFP standard requires that transceiver modules handle data rates of approximately 10 Gb/s, while outputting to the host through a serial interface among other things. Particularly, an XFI (10 Gb/s serial electrical interface) is designed for serial input from an XFP transceiver. This allows host designers and manufacturers to supply host systems assuming that XFP transceivers will perform the discussed functions.

[0010]     Therefore, it is desirable to provide a transceiver module capable of handling 10 Gb/s data input from a network within a jitter budget. It is further desirable to provide a transceiver module that interfaces with a host using serial connections, thereby allowing the

20600/06872/1343407

removal of SERDES components from the module. Additionally, it is desirable to provide

additional functionality, for example error monitoring functionality that is integrated within the

transceiver module that would identify errors and perform bit error rate tests ('BERTs') within a

data path and/or component on the module.

SUMMARY OF THE INVENTION

[0011]     The present invention overcomes the limitations of the prior art by providing

a transceiver module with eye diagram opening functionality for reducing jitter. In one

implementation, an optical transceiver module has a serial electrical interface with an electrical

output port and an electrical input port. The module also has a receive path and a transmit path.

The receive path includes an optical input port, a receiver eye opener and the electrical output

port of the serial electrical interface. An optical signal is received by the module at the optical

input port. The receiver eye opener retimes and reshapes a serial electrical data stream based on

the received optical signal. The retimed and reshaped serial electrical data stream is transmitted

from the module via the electrical output port. The transmit path includes the electrical input

port of the serial electrical interface, a transmitter eye opener and an optical output port. A

second serial electrical data stream is received by the module at the electrical input port. The

transmitter eye opener retimes and reshapes the received serial electrical data stream. An optical

signal based on the retimed and reshaped serial electrical data stream is transmitted from the

module via the optical output port.

[0012]     In one implementation, the receiver eye opener and the transmitter eye

opener are implemented in a single integrated circuit. The integrated circuit may also include

none, some or all of the following: digital to analog converters for example for converting

received digital signals to analog control signals, a bypass module for example for bypassing the

20600/06872/1343407

eye opener(s) under certain conditions, loopback data paths for example for performing

diagnostic tests, bit error rate (BERT) tester, adaptive equalizer(s) for example for conditioning

the serial data streams, power amplifier or other components for the receiver, driver (e.g., laser

driver) or other components for the transmitter, a control module and/or a serial control interface

for controlling the circuitry. The integrated circuit may also include various power down or

reduced power modes in order to conserve energy. In another aspect, the data path(s) may

include two or more eye openers, each suited for a different data rate. Switching between the eye

openers permits the accommodation of different data rates.

[0013]　　　Other aspects of the invention include applications, systems and methods

corresponding to the devices described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]　　　Fig. 1 is an illustration of a prior art transceiver module having a parallel

connection to a host.

[0015]　　　Fig. 2 is an illustration of a system including a transceiver module (e.g., an

XFP 10 Gb/s module) comprised of dual eye openers and having a serial connection to a host

according to an embodiment of the present invention.

[0016]　　　Fig. 3 is an example of an Integrated Circuit (IC) for providing eye opening

functionality to a receiver data path with a serial connection to a host.

[0017]　　　Fig. 4 is an example of an IC for providing eye opening functionality to a

transmitter data path with a serial connection to a host.

[0018]　　　Fig. 5 is an illustration of a transceiver module having dual eye openers

integrated on a single chip according to an embodiment of the present invention.

6

**[0019]** Fig. 6 is an illustration of a transceiver module having a communications path integrated with dual eye openers according to an embodiment of the present invention.

**[0020]** Fig. 7 is an illustration of a control module having a serial interface in a transceiver module having dual eye openers according to an embodiment of the present invention.

**[0021]** Fig. 8 is an example of an IC for providing dual eye opening functionality to a transceiver data path with a serial connection to a host.

**[0022]** Fig. 9 is an additional example of an IC for providing dual eye opening functionality to a transceiver data path with a serial connection to a host.

**[0023]** Fig. 10 illustrates a transceiver module comprising a DAC integrated on a chip with dual eye openers.

**[0024]** Fig. 11 illustrates a first DAC integrated into the receiver eye opener and a second DAC integrated into the transmitter eye opener.

**[0025]** Figs. 12A-D are block diagrams of loopback modes.

**[0026]** Figs. 13A-D are logic diagrams of loopback modes of an integrated chip with dual eye openers.

**[0027]** Fig. 14 is an illustration of a transceiver module with bypass functionality integrated with a transmitter and a receiver each having multiple CDR components according to an embodiment of the present invention.

**[0028]** Fig. 15 is a flowchart illustrating a first method bypass method operable in a transceiver module with an integrated transmitter and receiver, each having multiple CDRs.

[0029]     Fig. 16 is a flow chart of a second bypass method operable in a transceiver

module with a transmitter and a receiver each having multiple CDR components according to an

embodiment of the present invention.

[0030]     Fig. 17 is an embodiment of the bypass functionality of a dual eye opener IC

such as in Figs. 8 or 9.

[0031]     Fig. 18 is an illustration of a transceiver module having a BERT engine

integrated with dual eye openers according to an embodiment of the present invention.

[0032]     Fig. 19 is a flow chart of a BERT testing method operable in a transceiver

module having dual integrated eye openers.

[0033]     Figs. 20A-B illustrate embodiments of the BERT functionality of an

integrated chip with dual eye openers.

[0034]     Figs. 21A-B illustrate embodiments of an eye opener having an equalizer.

[0035]     Fig. 22 illustrates an embodiment of an equalizer according to the present

invention.

[0036]     Fig. 23 illustrates a coefficient module according to an embodiment of the

present invention.

[0037]     Fig. 24 illustrates a correlation module according to an embodiment of the

present invention.

[0038]     Figs. 25-27 illustrate examples of component integration that may be

implemented as part of an integrated circuit.

[0039]     Fig. 28 is an illustration of a transceiver module having power management

functionality integrated with dual eye openers according to an embodiment of the present

invention.

[0040]     Fig. 29 is a flow chart of a method for managing power of components on a transceiver module according to an embodiment of the present invention.

<u>DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS</u>

[0041]     An apparatus and method for providing serial connections between a transceiver module and host is described. In particular, clock and data recovery and error monitoring functionality is integrated on the transceiver module that allows these serial connections. One skilled in the art will recognize that embodiments of the present invention and description below may also be incorporated within a transponder module. In the following description, for purposes of explanation, specific details are set forth in order to provide an understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

[0042]     Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0043]     Fig. 2 is an illustration of a system including a transceiver module (e.g., an XFP 10 Gb/s module) comprised of dual eye openers and having a serial connection to a host according to an embodiment of the present invention. The receive path includes a receiver 215 coupled to a network and an eye opener 205. The eye opener 205 is designed to clean up high frequency jitter, e.g., "open" the eye diagram of serial data streams for optical transceivers. The receiver 215 includes a receiver optical sub-assembly ('ROSA') 235 that receives and converts

<div align="center">9</div>

an optical signal to an electrical signal. The receiver 215 also includes a post-amplifier 230 that amplifies the electrical signal to an appropriate power level. One skilled in the art will recognize that the eye opener 205b and ROSA may be manufactured and packaged using multiple methods. For example, the eye opener and ROSA may be integrated within a single ASIC or manufactured separately.

[0044]    The receiver eye opener 205b extracts a clock from the electrical signal and uses that recovered clock to regenerate degraded data within the signal. In particular, the receiver eye opener 205b provides retiming and reshaping that removes jitter (i.e., resets the jitter budget in the link). The retiming and reshaping function of the eye opener 205 may be implemented by a clock and data recovery ('CDR') and a retimer ('RT'), a signal conditioner, or any device capable of opening the eye diagram. Both passive and adaptive equalization circuits may be used for these purposes. The eye opener 205 is preferably responsive to the data rate of the data stream on the particular path. According to one embodiment, the receiver eye opener 205b includes a phase locked loop that aligns the phase of the electrical signal with a reference clock to ensure that the electrical signal is correctly clocked, and a signal shaper that filters noise from the signal and more accurately shapes the pulse edges in the signal. The eye openers 205a,b may be implemented as ASICs, as a configurable circuit such as an FPGA, or partly in software, to name but a few possibilities. One skilled in the art will recognize that there are numerous methods for providing eye opening functionality that operate in accordance with the present invention. After the electrical signal has been properly synchronized and shaped by the receiver eye opener 205b, it is transmitted to the host 105 via a serial path 260 such as an XFI-compliant 10 Gb/s transmission line.

[0045]     Other advantageous functions may also be implemented herein along with the eye openers 205a,b. In some embodiments, bypass, also known as "pass-through", functions are incorporated in the eye openers 205a, 205b which allow the data to bypass the retiming and reshaping functions of the eye opener. These bypass functions can be automatically selected, for instance by use of a loss of lock ('LOL') signal, or selectable with a control line or digital control. The eye openers 205a, 205b may also have low power modes (power down modes) that are enabled via a control pin, or by control through a digital bus or two wire interface. The eye openers 205a, 205b may also have BERT functions whereby a BERT engine within the eye opener generates data and/or an error detector matches up incoming data to a predetermined pattern to check for errors in the data stream. In addition, the eye openers 205a, 205b may have loopback functions that allow the data to be looped back with the addition of some signal I/Os between the eye opener. For instance, data from eye opener 205b may be routed over to eye opener 205a and this data transmitted to the transmitter 225 in place of the data from data path 250. In some combinations, these features allow the transceiver to perform self-test, or diagnostics of the data link, or diagnostics of the host system. These functionalities will be discussed in more detail below.

[0046]     The transmit path includes a transmitter 225 coupled to a network and a transmitter eye opener 205a. The transmitter eye opener 205a recovers degraded clock and data values from an electrical signal that travels from the host 105 via serial path 250 (e.g., 10 G/s transmission line). As described above, the electrical signal will degrade along this path 250 and the eye opener 205a compensates for this degradation and sends the electrical signal to the transmitter 225. The transmitter 225 includes a transmitter optical sub-assembly ('TOSA') 245 that converts an electrical signal to an optical signal and transmits it onto a network. The

transmitter 225 also preferably includes a laser driver 240 that controls a laser within the TOSA 245 and the modulation of data within the electrical signal onto the optical signal. The laser within the TOSA 245 is also biased to the proper operating current using a dedicated biasing and control circuit that may be contained within or outside of the laser driver. The transmitter 225 may include eye opener 205a depending on the particulars of the packaging and design chosen.

[0047] This transceiver module 200 allows serial connections 250, 260 between the transceiver module 200 and the host 105. In particular, the receiver and transmitter eye openers 205a, 205b compensate, on for signal degradation that occurs on these serial connections 250, 260 at high data rates, such as a data rate of about 10 Gb/s or higher.

[0048] Fig. 3 is an example of an integrated circuit ('IC') for providing eye opening functionality to a receiver data path with a serial connection to a host. The eye opener IC 205b includes a CDR 925b and an RT 935b. An input of the CDR 925b receives a data path from an output of a buffer 945d and a reference clock signal from an output of a buffer 945h. A buffer 945d, receives the data path from the network through a receiver 215. A buffer 945h, receives the reference clock signal from the host. The CDR 925b uses the reference clock as a starting point in recovering the data and clock signal from the data path. A clock multiplier unit may be used to adjust the rate of the reference clock as indicated by a rate select pin. The RT 935b is configured to retime and reshape the data path. A first input of RT 935b receives the data from a first output of the CDR 925b and a second input of the RT 935b receives the recovered clock signal from a second output of the CDR 925b.

[0049] The eye opener IC 205b provides a not ready signal to the host. One condition that activates the not ready signal is a result of a loss of signal ('LOS') signal. A first input of control logic 999b receives the LOS signal from an output of the buffer 945b when the

12                                                    20600/06872/1343407

buffer 945b does not detect incoming data. Another condition that activates the not ready signal as a result of a LOL signal. A second input of the control logic 999b receives the LOL signal from an output of CDR 925b when the CDR 925b is not able to lock onto the signal such as when the data rate is outside of the CDR 925b's range. The control logic may, for example, be implemented as OR gate logic.

[0050] A MUX 955b provides bypass functionality to the data path. The output of buffer 945b is coupled to a first input of the MUX 955b. A second input of the MUX 955b is the retimed and reshaped data output of RT 935b. The control logic 999b sends a control signal to the selector input of the MUX 955b to select either the first or second input. The control logic 999b selects the buffered data from buffer 945b in response to receiving a LOL, an LOS, or bypass signal (e.g., from the host). In this embodiment, the control logic 999b selects the output RT 935b as a default condition.

[0051] A polarity control coupled to the input of the buffer 945a changes the polarity of its output signal, which is preferably composed of differential signaling. Also, the buffer 945d is preferably a coupled mode logic buffer and the buffer 945h is preferably a positive emitter coupled logic buffer.

[0052] Fig. 4 is an example of an IC for providing eye opening functionality to a transmitter data path with a serial connection to a host. The eye opener IC 205a includes a CDR 925a and an RT 935a, each operating as described with respect to Fig. 3 except that the data flow is received from the network through a transmitter 225 and sent to the host. An input of the CDR 925a receives a data path from an output of a buffer 945a and a reference clock signal from an output of a buffer 945c. It will be understood that other components of the IC eye opener 205a may also be included in the eye opener IC 205a.

13

[0053]    The eye opener IC 205a includes control logic 999a to implement the not ready signal. A MUX 955a implements the bypass functionality.

[0054]    A MUX 955g allows the retimer 935a to retime the data in synchronization with a Tx clock provided, in one example, by the host. A first input of the MUX 955g receives a ref clock signal for use by the RT 925a as a starting point in retiming the data. A second input of the MUX 955g receives a Tx clock signal, which is preferably a high-quality signal that may be used for retiming the data in place of the recovered clock signal. The Tx clock frequency may be adjusted by a clock multiplier unit as indicated by a rate select pin. The MUX 955g selects between the ref clock signal and the Tx clock signal according to a clock select signal. In one embodiment, the clock select signal is transmitted over a serial line along with other signals instead of through a dedicated pin.

[0055]    Fig. 5 is an illustration of a transceiver module having dual eye openers integrated on a single chip according to an embodiment of the present invention. This integration allows a smaller aggregate board space to be used, in part, because the eye openers replace the relatively larger, more power hungry SERDES 110, 120 on the transceiver module. In some embodiments, the SERDES 110, 120 may be included on the host. Also, a higher density of transceivers can be placed in a line card. Furthermore, the packaging is simpler, and provided at a lower cost.

[0056]    In addition, the receiver eye opener 205b and the transmitter eye opener 205a can share the single reference clock 320. Accordingly, this integration reduces the number of inputs or pins on the chip itself, allows for easier testing of the chip, and reduces the number of components. Reference clock 320 is usually an input from the host board and is a clock at a sub-harmonic of the data rate. While it is possible to maintain the clock at exactly the data rate,

20600/06872/1343407

this may not be desirable for signal integrity and EMI reasons. Generally the reference clock is 1/16th or $1/64^{th}$ of the data rate. In some operating modes of the transceiver it would be possible to use the recovered clock from the receiver eye opener 205b as the reference clock of the transmitter eye opener 205a. Alternately, the reference clock input to eye opener 205b can be internally rerouted to act as the reference clock 320 for the receiver eye opener 205b. In either case, a reference clock 320 is still supplied by the host board.

[0057]     In other embodiments, the receiver 115, the transmitter 125, or portions thereof (e.g. post-amplifier or laser driver) may be integrated onto the chip as described below.

[0058]     Fig. 6 is an illustration of a transceiver module having a communications path integrated with dual eye openers according to an embodiment of the present invention. In particular, the chip may include an eye opener control module 350 that controls both the receiver eye opener 205b and the transmitter eye opener 205a. The eye opener control module 350 may be accessed and controlled by a user through a parallel connection, as shown, or a serial connection that is discussed below. Additionally, an eye opener communication module 340 may be integrated on the chip to facilitate intelligent communication between the receiver eye opener 205b and the transmitter eye opener 205a. For example, the eye opener communication module 340 may have direct connections to the receiver eye opener 205b and transmitter eye opener 205a enabling intelligent analysis and coordination between the two eye openers 205a,b. In another embodiment, the eye opener communication module 340 may have connections 360, 365, 370, 375 that allow it to tap data in front of and behind the receiver and transmitter eye opener. The embodiment would allow the eye opener communication module 340 to monitor both eye openers 205a,b detect a failing eye opener, and perform diagnostic tests in which data flow is altered to test an individual eye opener or data link.

[0059] Fig. 7 is an illustration of a control module having a serial interface in a transceiver module having dual eye openers according to an embodiment of the present invention. According to this embodiment, the eye opener control module 350 comprises a polarity control 379, a bypass control 377, a baudrate control 381, a clock polling control 383, a loopback control 387, a BERT control, and a serial interface 385. A clock polling control 385 allows the eye opener control module 350 to poll the clocking frequency on the receiver eye opener 205b and the transmitter eye opener 205a. A polarity control 379 allows the eye opener control module 350 to selectably control the input/output data polarity on the receiver eye opener 205b and the transmitter eye opener 205a. A baudrate control 381 allows the eye opener control module 350 to adjust the baudrate response of the receiver eye opener 205b and the transmitter eye opener 205a.

[0060] A pass-through control 377 allows the eye opener control module 350 to activate / deactivate the receiver eye opener 205b and the transmitter eye opener 205a to allow data streams that are incompatible with a data rate range of a particular eye opener to pass through the transceiver module 200. For example, if an eye opener is designed to retime a data stream of about 10 Gb/s, the bypass control 377 may automatically pass-through a 1 Gb/s data stream. Alternatively, the bypass control 377 may be manually controlled allowing a host 105 or network operator to determine whether to pass-through a particular data stream. A loopback control 387 allows the eye opener control module 350 to monitor the integrity of data paths and components on module 200. The BERT control 389 allows the eye opener control module 350 to test bit error rates of data paths and components on module 200. In other embodiments, additional controls to chip functions may be added to the eye opener control 350 such as an adaptive equalizer control.

16

[0061]     In one embodiment, a serial interface 385 allows a serial connection 390 to

communicate with the eye opener control module 350. In general, a serial connection such as

SPI, I2C, RS232, etc. may be used to control functions of the dual eye opener integrated

circuit 300. Other embodiments of serial connections are disclosed in U.S. Patent Application

No. 10/266,870, "Optical Transceiver Module with Multipurpose Internal Serial Bus," by Lewis

B. Aronson et al., filed October 8, 2002, which is incorporated by reference herein. Accordingly,

the number of pins required to command the eye opener control module 350 is reduced to a

single pin. For example, this serial interface 385 replaces four pins in a four rate configuration or

two pins in a binary rate configuration. In yet another embodiment, a second serial interface (not

pictured) may provide output to the host such as current polarity setting, a LOL signal, current

baudrate, a current clocking frequency, loopback test results, or BERT results. Alternatively, the

serial connection may be a single serial interface capable of facilitating two-way communication

between the eye opener control module 350 and the host.

[0062]     Fig. 8 is an example of an IC for providing dual eye opening functionality to

a transceiver data path with a serial connection to a host. The dual eye opener IC 300 includes an

eye opener 205a that receives a data from the host and sends a data to a transmitter, and an eye

opener 205b that receives a data from a receiver and sends a data to the host. Eye opener 205a

includes a CDR 925a and an RT 935a to perform reshaping and retiming as implemented in Fig.

9A. Eye opener 205a also has embodiments for providing a not ready signal to the host or bypass

functionality to the data path. Moreover, the eye opener 205b performs reshaping and retiming

the data with a CDR 925b and an RT 235b.

[0063]     The not ready signal output to the host from an output of a control logic

999b is conditioned upon receiving a LOS signal from an output of buffer 945d or a LOL signal

from an output of the CDR 925b. The MUX 955d provides bypass functionality. Bypass functionality is activated with a signal from the output of control logic 999b to a selector input of the MUX 955d. In another embodiment the Tx clock functionality may be implemented in the eye opener 205a.

[0064]     Fig. 9 is an additional example of an IC for providing dual eye opening functionality to a transceiver data path with a serial connection to a host. A MUX 975a provides an improved IC that includes both bypass and loopback functionality, along with other functionalities described above. If the first selector input of the MUX 975a receives the loopback signal, then the MUX 975a output switches to sending data received from the MUX 975b. If a second selector input of the MUX 975a receives the bypass signal from host or the LOL signal from the output of the CDR 925a, then the MUX 975a switches to sending data received from the output of the buffer 945a. The MUX 975a may be configured to implement either the loopback or the bypass when both selector inputs of the MUX 975a receive a signal. The MUX 975a replaces MUXs 955a, 955b, and 955c, thereby reducing the component count, saving power, and causing less heat dissipation.

[0065]     Fig. 10 illustrates a transceiver module comprising a DAC (digital to analog converter) on an integrated chip with dual eye openers. In this embodiment of dual eye opener IC 1020, a DAC 1025 converts digital signals sent through or from the IC 1020 to analog signals to control receiver and/or transmitter components. Accordingly, control signals sent to a post-amplifier 1030, a ROSA 1040, a laser driver 1050, and a TOSA 1060 can control characteristics such as analog swing, bias, and rise and fall times. In one embodiment, the digital signals sent to the DAC 1025 are generated by the control module 350 (see Figs. 6-7).

18                                             20600/06872/1343407

[0066]     Fig. 11 illustrates a first DAC integrated into the receiver eye opener and a

second DAC integrated into the transmitter eye opener. The DAC 1121 may control analog

signal outputs of the receiver eye opener 1122 or analog signal inputs from a receiver. Likewise,

the DAC 1123 may control analog signal outputs of the transmitter eye opener 1124 or analog

inputs from the transmitter as described with respect to Fig. 10.

[0067]     Figs. 12A-D illustrate loopback modes integrated with dual integrated eye

openers. A loopback mode allows an integrity check on a particular data path. Accordingly, a

first loopback mode may allow an integrity check of one or more components along the particular

data path on the module 200 or on an optical path on a network. A second loopback mode may

allow an integrity check of a data path containing multiple components on the module 200.

Thus, multi-mode loopbacks allow monitoring of data path integrity at different levels on the

transceiver module 200. The transceiver module 200 includes a eye opener loopback control 400

within a eye opener control 350 used to control the loopback functionality on the module 200.

[0068]     Fig. 12A illustrates a first loopback mode from the input 407 of the

transmitter eye opener 205a to the output 409 of the receiver eye opener 205b. This first

loopback 405 allows the host system 105 to check the function of the host board and check that

the transceiver module 200 is correctly plugged into its connector and is powered up properly.

Because this first loopback 405 is integrated within the module 200, an installer can quickly

determine whether the transceiver module 200 is properly installed or whether a failure occurred

within the transceiver module 200 or host 105.

[0069]     Fig. 12B is an illustration of a transceiver module having a second loopback

mode integrated with dual eye openers according to an embodiment of the present invention.

This second loopback 410 allows the host system 105 to check that the receiver eye opener 205b

20600/06872/1343407

is operating properly and that the transceiver module 200 is properly plugged into its connector and powered up properly. Because the second loopback 410 is integrated within the transceiver module 200, a manufacturer can quickly test the integrity of the receiver eye opener 205b prior to shipment as well as allowing a network administrator to easily check the receiver eye opener 205b after installation of the transceiver module 200.

[0070]	Fig. 12C is an illustration of a transceiver having a third loopback mode integrated with dual eye openers according to an embodiment of the present invention. This third loopback 420 allows the host system 105 to check that the transmitter eye opener 205a is operating properly and that the transceiver module 200 is properly plugged into its connector and powered up properly. Because the third loopback 420 is integrated within the transceiver module 200, a manufacturer can quickly test the integrity of the transmitter eye opener 205a prior to shipment as well as allowing a network administrator to easily check the transmitter eye opener 205a after installation of the transceiver module 200.

[0071]	Fig. 12D is an illustration of a transceiver module having a fourth and fifth loopback mode integrated with dual eye openers according to an embodiment of the present invention. The fourth loopback 425 is from the output 409 of the receiver eye opener 205b to the input 407 of the transmitter eye opener 205a. This fourth loopback 425 allows for testing of the transceiver module 200 and an optical data path on a network. Thus, a network administrator or module manufacturer can quickly test the entire transceiver module 200 and test whether the module 200 is properly coupled onto fiber. The fifth loopback 430 is from the output 409 of the receiver eye opener 205b to the output 417 of the transmitter eye opener 205a. This fifth loopback 430 allows for testing of the front end components on the transceiver module 200, the receiver eye opener 205b, and an optical data path on a network. A sixth loopback (not pictured,

but see Fig. 10B and Fig. 10D for IC implementation) is from the output 417 of the transmitter eye opener 205a to the input 412 of the receiver eye opener 205b.

[0072]    The above-described loopback modes are examples of loopbacks that may be integrated in the transceiver module 200 and is not meant to include all possible loopback modes.  For example, loopbacks may be integrated from the input 412 of the receiver eye opener 205b to both the input 407 and the output 417 of the transmitter eye opener 205a.  These loopbacks would allow testing of the front end components and an optical path as well a combination of front end components, the receiver eye opener 205a and an optical path.  Additional loopbacks may also be integrated within the transceiver module 200 to test other data paths and/or components.

[0073]    Referring to the example of Fig. 8, MUXs 955b, 955c, 955f, and 955g provide loopback functionality for testing components as described above.  In eye opener 205a, MUXs 955b and 955c receive a first loopback signal from the host to each selector input.  When the first loopback signal is high, the output of the MUX 955c switches from sending data received from the output of the CDR 925a to the input of the RT 925a to sending data received from the output of the CDR 925b to the input of the RT 925a.  At the same time, the output of the MUX 955b switches from sending the recovered clock signal received from the output of the CDR 925a to the input of RT 935a to sending the recovered clock signal received from the output of the CDR 925b to the input of RT 935b.

[0074]    In eye opener 205b, MUXs 955e and 955f receive a second loopback signal from the host to each selector input.  When the second loopback signal is high, the output of MUX 955f sends data received from the CDR 925a to the input of RT 935b rather than data from

CDR 925b, and a recovered clock signal received from the CDR 925a to the input of RT 935b rather than from the CDR 925a.

[0075] Fig. 13A is an embodiment of the third loopback mode of a dual eye opener IC such as in Fig. 12B. For the purposes of illustration, some components that are transparent to the data path during normal operation are omitted. The dual eye opener IC 300 includes eye opener 205a and eye opener 205b. In loopback mode, an input of a buffer 945a receives the data path from the host into eye opener 205a, and an input of a CDR 925a receives the data path from an output of the buffer 945a. In eye opener 205b, an input of an RT 935b receives the data path from an output of the CDR 925a, an input of a buffer 945e receive the data path from an output of the RT 935b and transmits the data path to back to the host.

[0076] In an alternative embodiment of the third loopback mode, the buffer 945a may be isolated by coupling the output of the buffer 945a to the output of the buffer 945e as in the first loopback mode. It will be understood that each of the other loopback modes may be similarly implemented. The second loopback mode may be implemented by coupling the input of the first CDR 925a or the input of the first buffer 945a to the output of the second CDR 925b or the input of the buffer 945a. The fourth loopback mode may be implemented by coupling the output of the second CDR 925b to the input of the first CDR 925b. The fifth loopback mode may be implemented by coupling the output of the second CDR 925b to the output of the first CDR 925a. The above-described loopback implementations are examples that are not meant to include all possible implementations.

[0077] Fig. 13B is an embodiment of the sixth loopback mode of a dual eye opener IC such as in Fig. 12B. An input of the receiver 215 receives the data path from the network. In the eye opener 205b, an input of a buffer 945d receives the data path from an output of a receiver

215, and an input of a CDR 925b receives the data path from an output of the buffer 945d. In the eye opener 205a, an input of a RT 935a receives the data path from an output of the CDR 925b, and an input of a buffer 945b receives the input from an output of the RT 935a. An input of a transmitter 225 receives the data path from an output of the buffer 945b and transmits the data path to the network. Other embodiments of the sixth loopback mode may be implemented where the data path is output from the eye opener 205b from a different component, such as the buffer 945d, and the data path is received in the eye opener 205a in a different component such as the buffer 945b.

[0078]    Fig. 13C is an embodiment of the third loopback mode data path of a dual eye opener such as in Fig. 12C. In the eye opener 205a, an input of a buffer 945a receives the data path from the host, an input of a CDR 925a receives the data path from an output of the buffer 945a, and an input of RT 935a receives the data path from an output of the CDR 935a. In the eye opener 205a, an input of a buffer 945e receives the input from an output of the RT 935a and transmits the data path back to the host.

[0079]    Fig. 13D is an embodiment of the sixth loopback mode data path of a dual eye opener such as in Fig. 12C. An input of a receiver 215 receives the data path from the network. In an eye opener 205b, an input of a buffer 945d receives the data path from an output of the receiver 215, an input of a CDR 925b receives the data path from an output of the buffer 945d, and an input of RT 935b receives the data path from an output of the CDR 935b. In an eye opener 205a, an input of a buffer 945b receives the input from an output of the RT 935b. An input of a transmitter 225 receives the data path from an output of the buffer 945b and transmits the data path to the network.

23

[0080]    Fig. 14 is an illustration of a transceiver module with bypass functionality

integrated with a transmitter and a receiver each having multiple CDR components according to

an embodiment of the present invention. A conventional eye opener operates properly on signals

within a small range of data rates. Typically, an eye opener will lock onto an incoming data

stream only at a certain data rate or within a narrow data rate range. Additionally, some eye

openers may be able to lock onto data at sub-harmonics of an operable data rate. However, at

other data rates where the eye opener is unable to lock onto the data, the output on the eye opener

is typically squelched. This limitation of conventional eye openers reduces the flexibility of a

transceiver module to operate in different network environments. In particular, conventional eye

openers preclude a protocol agnostic transceiver module, with eye opener functionality on chip,

that may operate in accordance with different types of protocols and data rates.

[0081]    The bypass functionality of the present invention allows an eye opener to

automatically pass data through if it is unable to lock onto the data because it is not in a particular

data rate band. In particular, the eye opener may be designed to pass-through a data stream

having a data rate such that clock and data recovery is not required to remain within an

acceptable jitter budget. For example, this pass-through functionality would allow a 10 Gb/s

Ethernet transceiver to operate in particular Fibre Channel environments where a eye opener is

not required. Additionally, the functionality allows debugging or engineering of a link to occur

without the presence of the non-linear regeneration feature of the eye opener. The pass-through

functionality of the eye opener may be automatically controlled depending on whether the eye

opener is locked to the data. The eye opener may generate a LOL signal which is a signal of

general use, but which can also be used for this purpose. The pass-through functionality may

also be externally controlled by a control signal or by a digital signal on a digital interface. It is

24                                    20600/06872/1343407

recognized that the bypass feature is valuable as a diagnostic and development tool even for data rates that are within the locking range of the eye opener.

[0082]     One embodiment of a transceiver module 200 having pass-through functionality, shown in Fig. 14, includes a receiver eye opener 205b, an eye opener 205a, and pass-through control 510 in the eye opener control module 350. Data received from the receiver is stored within a fourth buffer 945d in the receiver eye opener 205b without resetting a jitter budget within the data path. The fourth buffer 945d is coupled to a bypass line 532 and a first CDR 534. The pass-through control 510 toggles the output on the fourth buffer 945d between the pass-through line 532 and the first CDR 925a depending on whether the second CDR 925b can lock onto the data. The bypass control 510 may be designed to automatically toggle between the outputs on the fourth buffer 945d or be manually controlled by an operator via a control interface (e.g., serial interface 385). For example, a fourth CDR 925d may also be coupled to the fourth buffer 945d to operate on a different data stream than data operated on by the second CDR 925b. Also, this fourth CDR 925d would allow toggling by the pass-through control 510 between three different data paths. It will be understood that multiple eye openers may operate within the receiver eye opener 205b to facilitate different data streams being provided eye opener functionality on the eye opener 205b. Additionally, rate detection may be integrated along a receive path or transmit path to enable intelligent detection of data rates received from both a host and a network. According to one example, an adjustable wideband oscillator and logic circuitry may be used to identify a rate on a particular signal. In another example, multiple narrowband oscillators, a discriminator, and logic circuitry may also be used to identify the rate of a signal. This rate detection facilitates the use of multiple eye openers along a data path

resulting in eye opener functionality on a single data path being available to signals having different data rates.

[0083]    A similar bypass operation may be provided on the transmitter eye opener 205a. In particular, a first buffer 945a is coupled to a first CDR 925a and a pass-through line 526. The pass-through control 510 toggles data between the first CDR 925a and the pass-through line 526 depending on the characteristics of the data. Additionally, multiple eye openers (e.g., a third CDR 925c) may operate within the transmitter eye opener 205a to facilitate different data streams being provided eye opener functionality on the eye opener 205b.

[0084]    Fig. 15 is a flowchart illustrating a first method bypass method operable in a transceiver module with an integrated transmitter and receiver, each having multiple CDRs. A data rate of a data stream entering a eye opener is detected 540. In response to the detected data rate being outside a predefined range of operation of an eye opener, the data stream is passed through the transceiver module without eye opening 542. This bypass functionality may be automated on the CDR 1-IC or manually controlled by a user. In response to the detected data rate being within the predefined range of operation of an eye opener, eye opening is performed on the data stream to reduce jitter 545.

[0085]    Fig. 16 is a flow chart of a second bypass method operable in a transceiver module with a transmitter and a receiver each having multiple CDR components according to an embodiment of the present invention. A control signal is detected 550 by a buffer storing a data stream. In response to the control signal being in a first state (e.g., high), the data stream will be passed through a transceiver module without eye opening 552. In response to the control signal being in a second state (e.g., low), a eye opening is performed on the data stream 555.

20600/06872/1343407

[0086]     Fig. 17 is an embodiment of the bypass functionality of a dual eye opener IC such as in Figs. 8 or 9. The dual eye opener IC 300 includes an eye opener 205a and an eye opener 205b. Because the CDR and RT modules do not operate on the data path, a data from the host received into an input of the buffer 945a is sent directly from an output of the buffer 945a to an input of the buffer 945b. An output of the buffer 945b sends data path to an input of a transmitter 225 for transmission to the network. Likewise, data received from the network into an input of a receiver 215 and sent to from an output of the receiver 215 to an input of the buffer 945d is sent directly from an output of the buffer 945d to an input of the buffer 945e. An output of the buffer 945e sends the data to the host. A signal may be included for manual override of the bypass mode. The control signals necessary to activate bypass functionality are discussed above.

[0087]     In one embodiment, adaptive equalization is performed on signal by the host board during bypass mode for noise reduction and/or signal processing. The not ready signal may be polled to determine whether the eye opener is currently operating in bypass mode, initiating the adaptive equalization functionality when the not ready signal is high. The adaptive equalization feature advantageously compensates for link dispersion as a substitute for retiming and reshaping ordinarily provided by the eye opener.

[0088]     Fig. 18 is an illustration of a transceiver module having a BERT engine integrated with dual eye openers according to an embodiment of the present invention. According to one embodiment of the invention, a BERT engine 630 is integrated in a chip 600 having the transmitter eye opener 205a and the receiver eye opener 205b. The BERT engine 630 comprises a pattern generator 640, an error detector 635, and a BERT loopback control 650. In

another embodiment, the BERT engine 630 is integrated within the eye opener control module 350.

[0089] The BERT engine eye opener uses test points integrated within the data paths to inject and receive bit sequences that are used to test the bit error rate associated with particular paths. In this example, four test points are integrated on the transceiver module 200 and are identified as points A 605, B 610, C 615, and D 620. These test points 606, 610, 615, 620 allow the BERT engine 630 to inject and retrieve bit sequences on a data path. Using these test points, the BERT engine 630 may determine a bit error rate on external optical paths on an attached network, internal electrical paths or a combination of both electrical and optical paths.

[0090] The BERT engine 630 is useful both as a diagnostic function for end-customers in their systems, but is also useful as part of the module manufacturing process. For example, a manufacturer may perform integrity tests on the transceiver module 200 to ensure that the module passes a quality test. The BERT engine 630 may test internal paths on the module 200 during various operating conditions such as operating within a temperature chamber under temperature cycle or voltage margining. This feature provides a more efficient method of testing the module 200 when compared to more traditional external BERTs. Additionally, both the loopback modes and BERT engine 630 may operate in transponder modules as well.

[0091] Fig. 19 is a flow chart of a BERT testing method operable in a transceiver module having dual integrated eye openers. A bit sequence or test pattern is inserted 670 at a particular test point on the transceiver module 200. The bit sequence is output by the pattern generator 640. The pattern generator may use psuedo-random numbers and/or characters in the output or a pattern stored in a memory. The bit sequence travels along a path and is retrieved at another test point. Errors within the bit sequence are detected 675 and evaluated by the error

detector 635. This error rate testing and evaluation may occur under various environmental conditions 680 allowing the BERT engine 630 to test the module 600 at different environmental conditions 685 and retest the bit error rate of the path under a new condition. BERT engine 630 results may be sent to the host for evaluation.

[0092]     Fig. 21A illustrates a first embodiment of an eye opener having an equalizer. The data path of eye opener 2100 comprises an equalizer 2120, which receives data from a buffer 2105a and outputs data to a buffer 2105b. The buffer 2105a receives data from a receiver and the buffer 2105b sends data to a host. In another embodiment, the buffer 2105a receives data from the host and the buffer 2105b sends data to a transmitter. In one embodiment the eye opener 2100 conditions a signal in bypass mode.

[0093]     The equalizer 2120 resets the data path's jitter budget by reshaping and retiming the data to remove channel noise from sources such as inter-symbol interference. The equalizer 2120 is coupled to receive signals representing coefficients from a coefficient module 2110 and a clock signal from a CDR 2130. The equalizer 2120 is preferably an adaptive equalizer that adapts to channel conditions such as changing temperature, but in other embodiments, the equalizer 2120 may be a passive equalizer. Other embodiments of equalizers are disclosed in U.S. Patent Application No. 10/288,324, "System and Method for Reducing Interference in an Optical Data Stream," by Thomas J. Lenosky et al., filed on November 5, 2002; U.S. Patent Application No. 60/423,970, "System and Method for Reducing Interference in an Optical Data Stream Using Multiple Selectable Equalizers," by Thomas J. Lenosky et al. filed on November 5, 2002; and U.S. Patent Application No. __/_____, "Method And Apparatus For Reducing Interference in an Optical Data Stream Using Data-Independent Equalization," by Thomas J. Lenosky et al., filed on April 17, 2003; all of which are herein incorporated by

reference. The equalizer 2120 may comprise a feed forward filter having a finite impulse response, a DFE ('Decision Feedback Equalizer'), or the like, either alone or in combination. The output of the equalizer 2120 may be analog or digital, depending on the implementation. Further embodiments of the equalizer 2120 are discussed below.

[0094] The coefficient module 2110 provides coefficients to the equalizer 2120 by evaluating channel effects on the data. The coefficient module 2110 is coupled to receive the data from the buffer 2105a and send the coefficient signal to the equalizer 2120. The coefficient module 2110 may be implemented in hardware, software, or firmware. Further embodiments of the coefficient module 2110 are discussed below.

[0095] The CDR 2130 provides a clock to the equalizer 2120 by extracting a recovered clock signal from the data stream. The CDR 2130 is coupled to receive the data from the buffer 2105a and to send a clock signal to the equalizer 2120. One of ordinary skill in the art will recognize that the CDR 2130 may receive the data to recover the clock signal from other points in the data path such as at the equalizer 2120 output. Furthermore, the CDR 2130 may comprise the variations discussed herein.

[0096] Fig. 21B illustrates a second embodiment of an eye opener having an equalizer. In this embodiment, the data path of eye opener 2180 comprises an equalizer 2150 in series with a CDR 2160 coupled with an RT 2170. The equalizer 2150 receives data from the buffer 2155a and the RT 2170 outputs data to the buffer 2155b. The CDR 2160 and equalizer 2150 may be disposed on separate chips or an integrated circuit. One advantage of this embodiment, is that the signal is conditioned by both the equalizer 2150 and CDR 2160, leading to a lower bit error rate.

[0097]     In contrast to the embodiment of Fig. 21A, the equalizer 2150 preferably reshapes and outputs an analog signal by removing channel effects.  The equalizer 2150 receives a clock signal from the CDR 2160 to clock the equalizer's digital components.

[0098]     The CDR 2160 and RT 2170 retime and reshape the equalized data.  The RT 2170 receives a clock signal recovered by the CDR 2160.  The CDR 2160 and RT 2170 may comprise the variations discussed herein.

[0099]     In another embodiment, the equalizer 2150 is disposed on a first chip and the CDR 2160 and RT 2170 are disposed on a second chip.  The first chip may also comprise a CDR to clock the digital portions of the equalizer 2150 without relying on the CDR 2160 of the second chip.  Advantageously, by not traveling off-chip, the high-speed clock signal may remain low-powered and experience less degradation.

[0100]     Fig. 22 illustrates an equalizer according to an embodiment of the present invention.  A data path of the equalizer 2200 comprises a feed forward filter and a feedback path comprises a DFE.  The feed forward filter, receiving analog data from an input buffer, includes a plurality of delay lines 2210a-c, a plurality of multipliers 2230a-c, a summer 2250, and a slicer 2260.  The delay lines 2210a-c receive the data from the input buffer and the slicer 2260 sends the data to the output buffer.  The feed back path, receiving digital data from the summer 2250, includes the slicer 2260, a plurality of delay lines 2220a,b, and a plurality of multipliers 2240a,b.

[0101]     The delay lines 2210a-c, 2220a,b delay the data stream so that data bits are input at individual integrators at different clock cycles.  The delay lines 2210a-c, 2220a,b are coupled to receive an analog signal carrying either analog or digital data and send the data to the multipliers 2230a-c, 2240a,b.  The delay lines 2210a-c, 2220a,b may be implemented in various

ways such as through analog transmission lines comprising combinations of inductors and capacitors. Preferably, the delay is a one-bit period.

[0102]    The multipliers 2230a-c, 2240a,b generate a product of the data and coefficients. The multipliers 2230a-c, 2240a,b are coupled to receive the data signals and the coefficient signals and send to send a signal to the summer 2250. The summer 2250 generates a sum of the feed forward filter and the DFE. The summer 2250 is coupled to receive signals from the feed forward multipliers 2230a-c and from the DFE multipliers 2240a,b. The slicer 2260 receives the analog signal from the summer 2250 and a clock signal, and generates a digital output according to the clock signal.

[0103]    In one embodiment, the equalizer 2200 outputs a digital signal from the slicer 2260 output such as in the embodiment of Fig. 21A in which the equalized signal may receive no further conditioning before a data symbol decisions are made. In another embodiment, the equalizer 2200 outputs an analog signal from the summer 2250 output such as in the embodiment of Fig. 21B in which the equalized signal is input into a CDR.

[0104]    Fig. 23 illustrates a coefficient module according to an embodiment of the present invention. A data path of the coefficient module 2800 comprises a bank of correlation modules 2810a-c, an ADC logic 2820, a microcontroller 2830, and a DAC logic 2840. The bank of correlation modules 2810a-c receives data from an input buffer and the DAC logic 2840 outputs a coefficient signal to an equalizer or an output buffer.

[0105]    The bank of correlation 2810a-c modules performs autocorrelation functions on the data stream. The bank of correlation modules 2810a-c receive data signals from the input buffer and send signals to the ADC logic 2820. In Fig. 28, the bank of correlation modules 2810a-c calculates $<s(t)s(t+\delta)>$, $<s^2(t)s(t+\delta)>$, and $<s(t)s^2(t+\delta)>$ for $\delta = 1, 2, 3$, etc.

[0106]     The ADC logic 2820 digitizes analog signals from the bank of correlation modules 2810a-c and sends digital signals to the microcontroller 2830. The ADC logic 2820 comprises a multiplexor to multiplex multiple inputs on a single output. The microcontroller 2830 uses algorithms to determine coefficient values according to the autocorrelation results. The microcontroller 2830 comprises a memory element such as a EEPROM for storing instructions and past coefficient values. The DAC logic 2840 generates an analog signal from the digitized output of the microcontroller 2830.

[0107]     Fig. 24 illustrates a correlation module according to an embodiment of the present invention. The correlation module 2900 comprises a plurality of delay lines 2910a-d, a plurality of multipliers 2920a-c, and a plurality of integrators 2930a-c. The multipliers 2920a-c are preferably analog multipliers such as Gilbert cells and the integrators 2930a-c are preferably analog integrators. An advantage of the present invention is that analog circuitry determines correlations from the high-speed data input so that an output to ADC logic can be low-powered. Moreover, the correlation module 2900 generates coefficients without necessitating a training sequence.

[0108]     The correlation module 2900 is configured to calculate an autocorrelation function of the signal at different times, i.e., $<s(t)s(t+\delta)>$. A first data path includes a multiplier 2920a that receives inputs directly from the data stream and after a delay line 2910a and sends an output signal to an integrator 2930a. A second data path includes a multiplier 2920b that receives inputs directly from the data stream and after two delay lines 2910a,b and sends an output signal to an integrator 2930b. A third data path includes a multiplier 2920c that receives inputs directly from the data stream and after three delay lines 2910a-c and sends an output signal to an integrator 2930c. The number and types of data paths may vary according to specific

33

implementations within the scope of the present invention. The products are sent to a microcontroller.

[0109]     Figs. 25-27 illustrate examples of component integration that may be implemented as part of the integrated circuit, or within a transceiver module. Fig. 25 is an illustration of a transceiver module having amplification and laser components integrated with dual eye openers according to an embodiment of the present invention. This integration reduces the size of these components on the transceiver module 200 and allows for more efficient connections between the various components. The integration of additional circuits into the eye opener may also be desirable depending on the environment in which the eye opener will operate as well as obvious benefits such as reduced pin count, reduced package size and cost, reduced power consumption, improved signal integrity, etc. Also, additional control circuitry may be integrated within the eye opener. For instance, laser bias control circuitry, signal detect circuitry, and other circuits which might otherwise be incorporated into the postamp or laser driver separately.

[0110]     Figs. 26 and 27 illustrate other examples of component integration on a transceiver module. Specifically, the post amplifier 230 may be individually integrated with the dual eye openers 205a, b and the eye opener control module 350. Comparatively, the laser driver 240 may be individually integrated with the dual eye openers 205a, 205b and the eye opener control module 350. One skilled in the art that there are numerous additional implementations of component integration on a chip substrate in accordance with the present invention.

[0111]     The combinations of dual eye openers integrated with post amp and laser driver either singly or in combination may also be accomplished in the case of single eye openers 205a, b. Eye opener 205b can be integrated with the postamp or may have sufficient input

sensitivity to eliminate the requirement for a post amp. The eye opener 205b may also have signal detect features or other functions that may be incorporated into a post amp or used in a receiver. Likewise, the eye opener 205a may be integrated with the laser driver and with any other circuitry that is used in a transmitter, for example laser bias control circuitry. Eye opener 205a may have provisions for adjustable output swing, adjustable edge speed of the output, and other features that may be incorporated into laser drivers.

[0112] Fig. 28 is an illustration of a transceiver module having power management functionality integrated with dual eye openers according to an embodiment of the present invention. Control of power consumption may become significant, depending on the actual design, if multiple eye openers are implemented within the module 200. Accordingly, it is desirable to minimize the power consumption of components on the eye opener integrated circuit 800. Power down modes integrated in the eye opener integrated circuit 800 allow the eye opener control module 350 to power down components that are not being utilized during a particular time period. The power down modes may be externally controlled via control lines or digital interfaces, or they may be used automatically as part of the normal operation of the integrated circuit. For example, a signal detect function that may be active with a low duty cycle (e.g., 10%) so that the circuit, which would otherwise consume a substantial amount of current, will instead only consume 10% of the amount in the absence of automatic power down. The power down may occur on the scale of microseconds so that the circuit is turned on every few hundred microseconds, for example, and is powered down the rest of the time. Other signals within the eye opener might also be designed to utilize this type of power down. In addition, other circuits in the eye opener may be powered down when the eye opener is used in a transceiver module and these signals may be specific to use of the eye opener within a transceiver or transponder module.

The power down modes may also include a shutdown mode that turns off the eye opener in response to the absence of a signal for a particular period of time.

[0113]     In one embodiment, a component may operate on a duty cycle. For example, the circuitry necessary for the LOS may be powered up in response to a polling of the CDR. If the LOS condition exists, then the LOS signal is output. However, if the LOS condition does not exist, then a power savings is realized since the LOS will not be powered up again until the next polling.

[0114]     A power management module 805 within the eye opener control module 350 dynamically controls power levels on various components on the eye opener integrated circuit 800. For example, the power management module 805 may shut down the BERT engine 630 or pass-through control 510 if they are not being used. Additionally, the power management module 805 may decrease power to a eye opener (e.g., the receiver eye opener 205b or transmitter eye opener 205a) if it is not operating and may restore power to the eye opener when needed.

[0115]     In one embodiment, a host startup protocol module 810 within the eye opener control module 350 dynamically controls power levels on components during installation. For example, the host startup protocol module 810 may facilitate an initial handshaking procedure between the transceiver module 200 and the host 105. During installation, the transceiver module 200 may transmit a low power level inquiry to the host to request a start-up procedure. In response, the host 105 replies to the inquiry and the host startup protocol module 810 then powers up components on the transceiver module 200 needed to complete the setup procedure. Additionally the host 105 may communicate data describing whether its protocol operation of the dual eye openers.

20600/06872/1343407

[0116]    The power management module 805 and host startup protocol module 810

allow components on the transceiver module 200 to operate in a sleep mode when not in use. As

a result, power management efficiency is increased and heat on the chip is reduced.

[0117]    Fig. 29 is a flow chart of a method for managing power of components on a

transceiver module according to an embodiment of the present invention. In particular, a mode

of operation is determined 850 such as a mode not requiring a BERT engine. In response,

components not required for this mode may be powered down 860 such as a BERT engine for the

mode of operation in the example above.

[0118]    The present invention provides several benefits over conventional

transceiver modules. A first benefit is that is may be used to improve the performance of XFP

transceiver modules. XFP transceiver modules are small form factor optical modules operating

at a data rate of approximately 10 Gb/s.

[0119]    Another benefit of the present invention is that the transceiver module may

be plugged into serial connectors on a host reducing the number of SERDES components on both

the host and transceiver module. Dual eye openers may be placed in the transmit and receive

paths to ensure that data streams remain within a predefined jitter budget. The removal of

SERDES components decreases the amount of heat on the transceiver chip(s), decreases the

component cost, and reduces the required area on a chip substrate for components.

[0120]    An additional benefit of the present invention is that particular

functionalities may be integrated on the transceiver module. A first functionality is providing

control of various components, including dual eye openers, via a serial connection. This serial

connection reduces the number of pins and connections required to control the transceiver

module. A second functionality is providing multiple loopback modes that may be used to test

20600/06872/1343407

components and data paths on both the transceiver module and optical paths on an attached

network. Furthermore, a BERT engine may be integrated on the module to further enhance this

testing and monitoring capability of the loopback modes. These functionalities lower the

manufacturing costs and installation costs because the internal testing described above provides

more efficient and cost effective methods of testing than conventional testing procedures.

[0121]     Still yet another benefit of the present invention is that a pass-through

functionality may be integrated on the transceiver module. This pass-through function allows the

transceiver module to operate in different networking environments having different data rates

and eye opener requirements.

[0122]     The present invention may also include power management functionality

that is integrated on the transceiver module. This power management function allows the

dynamic control of power to components on the module during both operation and installation.

As a result, power is conserved and heat reduced on the chips.

[0123]     While the present invention has been described in detail in regards to a

transceiver, it will be understood from the above description that embodiments of the present

invention may be applied to a transponder as well.

[0124]     While the present invention has been described with reference to certain

preferred embodiments, those skilled in the art will recognize that various modifications may be

provided. For example, other types of circuits may be used to reduce jitter or open an eye

diagram at a transceiver or transponder module. For example, both passive and adaptive

equalization circuits may be used for these purposes. Also, one skilled in the art will recognize

that the above description may apply to reclocking circuitry as well. Accordingly, the

functionalities described above are not meant to be limited to an eye opener, but may be used in a

20600/06872/1343407

number of circuits used to improve a signal such as signal conditioners or eye openers.

Variations upon and modifications to the preferred embodiments are provided for by the present invention, which is limited only by the following claims.

20600/06872/1343407